WHAT IS CLAIMED IS:

1. A system comprising:

a clock control module;

a first functional unit; and

a second functional unit;

wherein the clock control module is configured to provide a first clock signal having a first frequency to the first functional unit in response to receiving a start signal, wherein the clock control module is configured to provide the first clock signal to the second functional unit in response to receiving a first control signal from the first functional unit, and wherein the clock control module is configured to stop providing the first clock signal to the first functional unit in response to receiving the first control signal from the first functional unit.

2. The system of claim 1 further comprising:

a third functional unit;

wherein the clock control module is configured to provide the first clock signal to the third functional unit in response to receiving a second control signal from the second functional unit, and wherein the clock control module is configured to stop providing the first clock signal to the second functional unit in response to receiving the second control signal from the second functional unit.

3. The system of claim 1 further comprising:

a third functional unit;

wherein the clock control module is configured to provide a second clock signal having a second frequency to the third functional unit in response to receiving a second control signal from the second functional unit, wherein the first frequency differs from the second frequency, and wherein the clock control module is configured to stop providing the first clock signal to the second functional unit in response to receiving the second control signal from the second functional unit.

4. The system of claim 1 wherein the clock control module is configured to stop providing the first clock signal to the second functional unit in response to receiving a second control signal from the second functional unit.

5. The system of claim 4 wherein the clock control module is configured to provide a second clock signal having a second frequency to the second functional unit subsequent to receiving the second control signal and in response to receiving a hibernate signal, and wherein the first frequency is greater than the second frequency.

6. The system of claim 5 further comprising:
a first clock configured to provide the first clock signal; and
a second clock configured to provide the second clock signal.

7. The system of claim 5 further comprising:
a control circuit configured to provide the start signal and the hibernate signal to the clock control module.

8. A system comprising:
a photo array;
an analog-to-digital converter coupled to the photo array;
a processor coupled to the analog-to-digital converter; and
a clock control circuit coupled to the analog-to-digital converter and the processor;
wherein the clock control circuit is configured to provide a first clock signal having a first frequency to the analog-to-digital converter in response to receiving a start signal, wherein the clock control circuit is configured to provide the first clock signal to the processor in response to receiving a first control signal from the analog-to-digital converter, and wherein the clock control circuit is configured to stop providing the first clock signal to the analog-to-digital

converter in response to receiving the first control signal from the analog-to-digital converter.

9. The system of claim 8 wherein the clock control circuit is configured to stop providing the first clock signal to the processor in response to receiving the second control signal from the processor, wherein the clock control circuit is configured to provide a second clock signal having a second frequency to the processor in response to receiving a hibernate signal, and wherein the first frequency is greater than the second frequency.

10. The system of claim 9 further comprising:

a control circuit coupled to the processor and the clock control circuit;

wherein the control circuit is configured to generate the start signal in response to receiving a third control signal from the processor, wherein the control circuit is configured to provide the start signal to the clock control circuit, wherein the control circuit is configured to generate the hibernate signal in response to receiving a fourth control signal from the processor, and wherein the control circuit is configured to provide the hibernate signal to the clock control circuit.

11. The system of claim 10 wherein the processor comprises:

a first circuit configured to receive digital frame information from the analog-to-digital converter;

a second circuit configured to process the digital frame information; and

a navigation circuit configured to generate the third and fourth control signals;

wherein the clock control circuit is configured to provide the first clock signal to the first circuit in response to receiving the first control signal from the analog-to-digital converter, wherein the clock control circuit is configured to provide the first clock signal to the second circuit in response to receiving a fifth control signal from the first circuit, wherein the clock control circuit is configured to stop providing the first clock signal to the first circuit in response

to receiving the fifth control signal from the first circuit, wherein the clock control circuit is configured to provide the first clock signal to the navigation circuit in response to receiving a sixth control signal from the second circuit, wherein the clock control circuit is configured to stop providing the first clock signal to the second circuit in response to receiving the sixth control signal from the second circuit, and wherein the clock control circuit is configured to stop providing the first clock signal to the navigation circuit in response to receiving a seventh control signal from the navigation circuit.

12. The system of claim 11 wherein the control circuit is configured to generate the hibernate signal in response to receiving the fourth control signal from the navigation circuit, and wherein the clock control circuit is configured to provide the second clock signal to the navigation circuit in response to receiving the hibernate signal.

13. The system of claim 9 further comprising:

a first clock coupled to the clock control circuit; and

a second clock coupled to the clock control circuit;

wherein the first clock configured to provide the first clock signal to the clock control circuit, and wherein the second clock configured to provide the second clock signal to the clock control circuit.

14. The system of claim 8 further comprising:

a motion register coupled to the processor;

wherein the processor is configured to store first information in the motion register, and wherein the first information is associated with second information generated by the photo array.

15. A method comprising:

providing a first clock signal having a first frequency to a first functional unit;

receiving a first control signal from the first functional unit subsequent to providing the first clock signal to the first functional unit;

providing the first clock signal to a second functional unit in response to receiving the first control signal; and

not providing the first clock signal to the first functional unit in response to receiving the first control signal.

16. The method of claim 15 further comprising:

receiving a start signal; and

providing the first clock signal to the first functional unit in response to receiving the start signal.

17. The method of claim 15 further comprising:

not providing the first clock signal to the second functional unit in response to receiving a second control signal from the second functional unit; and

providing a second clock signal having a second frequency that is less than the first frequency to the second functional unit subsequent to not proving the first clock signal to the second functional unit.

18. The method of claim 15 further comprising:

receiving a hibernate signal; and

providing the second clock signal to the second functional unit in response to receiving the hibernate signal.

19. The method of claim 15 further comprising:

providing the first clock signal to the first functional unit to cause the first functional unit to convert analog frame information from a photo array to digital frame information and provide the digital frame information to the second functional unit; and

providing the first clock signal to the second functional unit in response to receiving the first control signal to cause the second functional unit to process the digital frame information.

20. A wireless mouse comprising:

a navigation sensor comprising:

a photo array;

an analog-to-digital converter coupled to the photo array;

a processor coupled to the analog-to-digital converter; and

a clock control circuit coupled to the analog-to-digital converter and the processor; and

a wireless transceiver coupled to the navigation sensor;

wherein the clock control circuit is configured to provide a first clock signal having a first frequency to the analog-to-digital converter in response to receiving a start signal to cause the analog-to-digital converter to convert analog frame information from the photo array to digital frame information and provide the digital frame information to the processor, wherein the clock control circuit is configured to provide the first clock signal to the processor in response to receiving a first control signal from the analog-to-digital converter to cause the processor to generate position information using the digital frame information and provide the position information to the wireless transceiver, wherein the clock control circuit is configured to stop providing the first clock signal to the analog-to-digital converter in response to receiving the first control signal from the analog-to-digital converter, and wherein the wireless transceiver is configured to transmit the position information.

21. The wireless mouse of claim 20 wherein the clock control circuit is configured to stop providing the first clock signal to the processor in response to receiving the second control signal from the processor, wherein the clock control circuit is configured to provide a second clock signal having a second frequency to the processor in response to receiving a hibernate signal, and wherein the first frequency is greater than the second frequency.

22. The wireless mouse of claim 20 wherein the navigation sensor further comprises a motion register coupled to the processor, and wherein the processor is configured to store the position information in the motion register.